IN THE CLAIMS:

--1. (Currently Amended) A data processing circuit utilized for a serial interface comprising:

a receiving circuit coupled to an application side which receives as input a plurality of packet data of a plurality of channels therefrom;

a selection circuit having a channel identification data extracting circuit for extracting channel identification data regarding a number of selected channels ~~channel~~ in said input packet data, ; a comparison circuit for comparing said extracted channel identification data with channel specifying data ~~regarding a predetermined selected channel~~, and a packet data validity instruction signal generation circuit for outputting a packet data validity instruction signal indicating whether said packet data is valid or not based on a result of the comparing; and

a transmission circuit for providing said input packet data to a data transmission path when said packet data validity instruction signal is valid,

wherein the selection circuit is operable to ~~select as many as~~ extract two channels of data simultaneously from among the plurality of channels.--

--2. (Original) A data processing circuit as set forth in claim 1, wherein said channel identification data extraction circuit receives as input a packet data input timing signal for specifying an input timing of said packet data from said application side and extracts channel identification data regarding a selected channel in said input packet data based on said packet data input timing signal.--

--3. (Original) A data processing circuit as set forth in claim 1, wherein said transmission circuit transmits insert data to said data transmission path at a timing indicating that said packet data validity instruction signal is invalid.--

4. (Original) A data processing circuit as set forth in claim 3, wherein said insert data is information data regarding said selected channel.--

B1 amd.

--5. (Original) A data processing circuit as set forth in claim 1, further comprising a memory circuit for storing said channel specifying data.--

--6. (Original) A data processing circuit as set forth in claim 5, further comprising a computer for writing said channel specifying data to said memory circuit.--

--7. (Original) A data processing circuit as set forth in claim 1, further comprising:

a transmission packet data memory circuit for storing packet data to be transmitted to said data transmission path;

wherein said transmission circuit selects said input packet data and writes it to a transmission packet data memory circuit when said packet data validity instruction signal indicates validity.--

--8. (Original) A data processing circuit as set forth in claim 1, wherein said transmission circuit transmits said selected packet data to said data transmission path at predetermined intervals.--

B1 Cont.

--9. (Original) A data processing circuit as set forth in claim 1, wherein said data transmission path is a serial bus.--

--10. (Previously Presented) A data processing circuit as set forth in claim 1, wherein the serial interface is a 1394 serial interface.--

--11. (Canceled)